Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for testing a high-speed circuit having a first frequency of greater than one GHz, the high-speed circuit being a high-speed phase and clock recovery circuit, the method comprising the steps of:

obtaining a high-speed statistical signature of the high-speed circuit using a tester having a second frequency of not greater than one GHz, the tester being external to the high-speed circuit;

comparing the high-speed statistical signature of the high-speed circuit to an expected signature.

2. (Currently Amended) The method of claim 1 ~~wherein the high-speed circuit is a high-speed phase and clock recovery circuit and~~ wherein the high-speed statistical signature-obtaining step further includes the steps of:

utilizing the tester to provide a signal to the high-speed phase and clock recovery circuit, the signal having a delay corresponding to a phase change; and

reading an output signal from the high-speed phase and clock recovery circuit;

repeating the utilizing and reading steps a particular number of times.

3. (Original) The method of claim 2 wherein the high-speed statistical signature obtaining step further includes the step of:

performing the utilizing, reading and repeating steps again for at least a second delay.

4. (Original) The method of claim 2 wherein the utilizing step further includes the step of:

setting the delay using the tester.

5. (Original) The method of claim 2 wherein the high-speed phase and clock recovery circuit includes an internal data recovery phase setting, and wherein the utilizing step further includes the step of:

determining the delay using the internal data recovery phase setting.

6. The method of claim 2 wherein the high-speed phase and clock recovery circuit further includes at least one latch and wherein the output signal reading step further includes the step of:

reading sampled data from at least one oversampled latch.

7. (Original) The method of claim 2 wherein the high-speed phase and clock recovery circuit further includes a parallel bus and wherein the output signal reading step further includes the step of:

reading sampled data from the parallel bus.

8. (Original) The method of claim 1 wherein the high-speed circuit is a high-speed phase and clock recovery circuit and wherein the high-speed statistical signature-obtaining step further includes the steps of:

utilizing the tester to provide a signal to the high-speed phase and clock recovery circuit, the signal having a delay corresponding to a phase change;

reading an output signal from the high-speed phase and clock recovery circuit;

providing at least one new delay; and

repeating the utilizing and reading steps for the at least one new delay.

9. (Original) The method of claim 8 further comprising the steps of:

repeating the utilizing, reading, providing and repeating steps a particular number of times.

10. (Original) The method of claim 1 wherein the comparing step further includes the step of:

subtracting the high-speed statistical signature from the expected signature to obtain a difference between the high-speed statistical signature and the expected signature.

11. (Original) The method of claim 10 further comprising the step of:

determining whether the high-speed circuit passes the test based upon the difference being less than a particular amount at at least one selected portion of the high-speed statistical signature.

12. (Original) The method of claim 11 further comprising the step of:

repeating the high-speed statistical signature obtaining and comparing steps for at least one additional setting of the high-speed circuit.

13. (Currently Amended) A method for testing a high-speed circuit having a first frequency of greater than one GHz, the method comprising the steps of:

utilizing a tester to provide a signal to the high-speed phase and clock recovery circuit, the signal having a delay corresponding to a phase change, the tester having a second frequency of not greater than one GHz; and

reading an output signal from the high-speed phase and clock recovery circuit;

repeating the utilizing and reading steps a particular number of times;

performing the utilizing, reading and repeating steps again for at least a second delay;

comparing the high-speed statistical signature of the high-speed phase and clock recovery circuit to an expected signature to determine whether the high-speed phase recover circuit operates as desired; and

optionally repeating the high-speed statistical signature obtaining and comparing steps for at least one additional setting of the high-speed circuit.

14. (Original) The method of claim 13 wherein the comparing step further includes the step of:

subtracting the high-speed statistical signature from the expected signature to obtain a difference between the high-speed statistical signature and the expected signature.

15. (Currently Amended) A system for testing a high-speed circuit having a first frequency of greater than one GHz, , the high-speed circuit being a high-speed phase and clock recovery circuit, the system comprising:

a tester for providing at least one signal to the high-speed circuit, the tester having a second frequency of not greater than one GHz, the tester being external to the high-speed circuit;

at least one computer system, coupled with the tester, for obtaining a high-speed statistical signature of the high-speed circuit using the tester and for comparing the high-speed statistical signature of the high-speed circuit to an expected signature.

16. (Currently Amended) The system of claim 15 ~~wherein the high-speed circuit is a high-speed phase and clock recovery circuit and~~ wherein the at least one signal has a delay corresponding to a phase change, wherein the tester further reads at least one output signal from the high-speed phase and clock recovery circuit a particular number of times to provide statistical data for the high-speed statistical signature.

17. (Original) The system of claim 16 wherein the tester further provides the at least one signal, reads the at least one output signal the particular number of times for at least a second delay.

18. (Original) The system of claim 16 wherein the tester further sets the delay.

19. (Original) The system of claim 16 wherein the high-speed phase and clock recovery circuit includes an internal data recovery phase setting that is used to set the delay.

20. (Original) The system of claim 16 wherein the high-speed phase and clock recovery circuit further includes at least one latch and wherein the tester further receives sampled data from at least one oversampled latch.

21. (Original) The system of claim 16 wherein the high-speed phase and clock recovery circuit further includes a parallel bus and wherein the tester further receives sampled data from the parallel bus.

22. (Original) The system of claim 15 wherein the high-speed circuit is a high-speed phase and clock recovery circuit and wherein the at least one signal has a delay corresponding to a phase change, wherein the tester further sweeps the delay to provide a plurality of delays and reads at least one output signal from the high-speed phase and clock recovery circuit at at least a portion of the plurality of delays.

23. (Original) The system of claim 15 further comprising means for repeating the utilizing, reading, providing and repeating steps a particular number of times.

24. (Original) The system of claim 15 wherein the computer system further subtracts the high-speed statistical signature from the expected signature to obtain a difference between the high-speed statistical signature and the expected signature.